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**UTILITY PATENT
APPLICATION TRANSMITTAL**(Only for new nonprovisional applications
under 37 CFR 1.53(b))

Attorney Docket No.

991387

Total Pages

First Named Inventor or Application Identifier

Shigeo OHSAKA, Shinichi DOMOTO and Nobumasa OKADA

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APPLICATION ELEMENTS FOR:

**ELECTRODE STRUCTURE, PROCESS FOR
FABRICATING ELECTRODE STRUCTURE AND
SEMICONDUCTOR LIGHT-EMITTING DEVICE**ADDRESS TO: Assistant Commissioner for Patents
BOX PATENT APPLICATIONS
Washington, D.C. 202311639 U.S. PTO
09/456531

12/08/99

1. ☒ Fee Transmittal Form (Incorporated within this form)
(Submit an original and a duplicate for fee processing)2. ☒ Specification Total Pages [34]3. ☒ Drawing(s) (35 USC 113) Total Sheets [14]4. ☒ Oath or Declaration Total Pages [5]a. ☒ Newly executed (original)b. ☐ Copy from prior application (37 CFR 1.63(d)
(for continuation/divisional with Box 17 completed).i. ☐ Deletion of Inventor(s)Signed statement attached deleting inventor(s) named in prior application,
see 37 CFR 1.63(d)(2) and 1.33(b).5. ☐ Incorporation by reference (useable if box 4b is checked)The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under
Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby
incorporated by reference therein.6. ☐ Microfiche Computer Program (Appendix)7. ☐ Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)a. ☐ Computer Readable Copyb. ☐ Paper Copy (identical to computer copy)c. ☐ Statement Verifying identity of above copies**ACCOMPANYING APPLICATION PARTS**8. ☒ Assignment Papers (cover sheet and document(s))9. ☐ 37 CFR 3.73(b) Statement (when there is an assignee) ☒ Power of Attorney

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10. ☐ English translation Document (if applicable)

11. ☐ Information Disclosure Statement ☐ Copies of IDS Citations

12. ☒ Preliminary Amendment

13. ☒ Return Receipt Postcard (MPEP 503)

14. ☐ Small Entity Statement(s) ☐ Statement filed in prior application
Status still proper and desired.

15. ☒ Claim for Convention Priority ☐ Certified copy of Priority Document(s)

a. Priority of _____ application no. _____ filed on _____ is claimed under 35 USC 119.

The certified copies/copy have/has been filed in prior application Serial No. _____.

(For Continuing Applications, if applicable).

16. ☐ Other _____

17. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information:

☐ Continuation ☐ Division ☐ Continuation-in-part (CIP) of prior application no. ____/____

FEE TRANSMITTAL	Number Filed	Number Extra	Rate	Basic Fee
The filing fee is calculated below				\$760.00
Total Claims	18 - 20		x \$18.00	
Independent Claims	6 - 3	3	x \$78.00	234.00
Multiple Dependent Claims			\$260.00	
Basic Filing Fee				994.00
Reduction by 1/2 for small entity				
Fee for recording enclosed Assignment			\$40.00	40.00
TOTAL				\$1034.00

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[XX] A check in the amount of \$ 1,034.00 is enclosed to cover the filing fee of \$994.00 and the assignment recordation fee of \$40.00.

[] Please charge our Deposit Account No. **01-2340** in the total amount of _____ to cover the filing fee and the _____ assignment recordation fee. A duplicate of this sheet is attached.

[XX] The Commissioner is hereby authorized to charge payment for any additional filing fees required under 37 CFR 1.16 or credit any overpayment to Deposit Account No. **01-2340**. A duplicate of this sheet is attached.

18. CORRESPONDENCE ADDRESS

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Date: December 8, 1999

MRQ/yap

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **Shigeo OHSAKA et al.**

Serial Number: **Not Yet Assigned**

Filed: **December 8, 1999**

For: **ELECTRODE STRUCTURE, PROCESS FOR FABRICATING ELECTRODE
STRUCTURE AND SEMICONDUCTOR LIGHT-EMITTING DEVICE**

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

December 8, 1999

Sir:

Prior to the calculation of the filing fees of the above application, please amend the application as follows:

IN THE CLAIMS:

In each of claims 7, 8, 9, 10, 11 and 12, line 2, delete "any one of".

REMARKS

The above amendment is believed to place the claims in proper condition for examination.

Early and favorable action is awaited.

66001.125460

In the event there are any additional fees required, please charge our Deposit Account No.

01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN, HATTORI,
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ELECTRODE STRUCTURE, PROCESS FOR FABRICATING ELECTRODE
STRUCTURE AND SEMICONDUCTOR LIGHT-EMITTING DEVICE

BACKGROUND OF THE INVENTION

The present invention relates to an electrode structure, a process for fabricating the electrode structure and a semiconductor light-emitting device, more specifically an electrode structure having a parasitic capacity reduced with respect to a lower layer, a process for fabricating the electrode structure and a semiconductor light-emitting device.

These days, optical communication using semiconductor lasers, which enable high-speed and large-capacity information transmission, having been noted. A semiconductor laser generally has a structure including electrodes formed respectively on the upper sides and the back sides of the devices. Bonding pads are connected to the electrodes on the upper sides, and bonding wires are connected to the bonding pads. Modulation signals are supplied to the modulator region of the semiconductor laser.

Recently, further increase of the communication speed is required to meet larger capacities for information processing amounts. For higher communication speed it is necessary to use signal of radio-frequencies as the modulation signals.

However, in order that the modulation signals further have radio-frequencies, parasitic capacities between the bonding pads and the lower layer must be decreased. Delays in rises and falls of waveforms are caused corresponding to parasitic capacities between the bonding pads and the lower layer. In a case that the modulation signals have radio-frequencies, response delays due to parasitic capacities between the bonding pads and the lower layer become unnegligible.

In order to decrease parasitic capacities between the bonding pads and the lower layer it is proposed that the bonding pads have small areas. The bonding pads have small areas, whereby parasitic capacities between the bonding pads and the lower layer can be small.

However, there is a limitation to decreasing the bonding pad area. That is, the bonding pads requires a certain area for the bonding wires to be jointed to the bonding pads. When an area for the bonding is taken into account, the bonding pads cannot be made smaller than a certain area. Resultantly, parasitic capacities between the bonding pads and the lower layer cannot be decreased to about 1 pF. In a case of 1 pF, a modulation frequency could be increased to only about 2.5 GHz. Recently, the modulation speed is required to be increased to about 10 GHz. However, the modulation speed increase to about 10 GHz cannot be attained by decreasing the bonding pad area.

SUMMARY OF THE INVENTION

An object of the present invention is to provide an electrode structure which enables decrease of parasitic capacities with respect to a lower layer, a process for fabricating the electrode structure and a semiconductor light-emitting device using radio-frequencies.

In order to make a parasitic capacity between the bonding pads and a lower layer small it is proposed that a thick insulation film is formed below the bonding pads.

However, in a case that silicon oxide film or others is formed thick below the bonding pads, the silicon oxide film or others is broken due to a force applied upon the bonding, and the bonding pad peel off.

Then, it is proposed that polyimide layer, which is not broken easily even by a strong force and can be formed thick is formed below the bonding pads. It is considered that the polyimide layer will not be broken by impacts applied upon the bonding because polyimide is a material having high flexibility. A semiconductor laser including a polyimide layer formed thick below the bonding pads will be explained with reference to FIG. 14.

As shown in FIG. 14, a silicon nitride film 134 is formed on a substrate 110. A thick polyimide layer 136 is formed on the silicon nitride film 134. A silicon nitride film 138 is formed on the upper surface and the side surface of the polyimide layer 136.

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In the semiconductor laser shown in FIG. 14, the silicon nitride films 134, 138 cover the backside surface, the side surface and the upper surface of the polyimide layer 136 because the polyimide layer 136 has low adhesion to the lower layer and has high hygroscopicity. In the semiconductor laser shown in FIG. 14, the polyimide layer 136 has the back side surface, and side surface and the upper surface covered with the silicon nitride films 134, 138, whereby the polyimide layer 136 can have good adhesion to the lower layer, and the polyimide layer 136 can be prohibited from absorbing water. A bonding pad 124 is formed on the silicon nitride film 138.

However, in a case that the polyimide layer 136 is formed below the bonding pad 124 as shown in FIG. 14, the polyimide layer 136 is distorted due to an impact which is as large as, e.g., 500 kg/cm^2 applied to the polyimide layer 136 upon the bonding. The silicon nitride film 138 is accordingly broken. Good adhesion cannot be obtained any more between the broken silicon nitride film 138 and the bonding pad 124. As a result, the bonding pad 124 peels off the silicon nitride film 138. Thus, simply forming the thick polyimide layer 136 below the bonding pad 124 cannot make the semiconductor laser reliable.

Then, the inventors of the present application made earnest studies and have obtained an idea of art that the polyimide layer formed thick can stand impacts applied upon

the bonding.

The above-described object is achieved by an electrode structure including a conductive film formed on a base substrate through an insulation film, the insulation film comprising a plurality of poles of polyimide, a first film formed on side surfaces of the poles and formed of an insulation material having a higher hardness than polyimide, and a second film of polyimide buried among said a plurality of poles with the first film formed on the side surfaces thereof. Because of the first film of an insulation material having high hardness formed on the side surfaces of the poles of polyimide, even when a strong force is applied upon the bonding, the poles are prevented from being distorted, and the conductive film is protected from peeling off. Because of the thick polyimide layer below the conductive film, a parasitic capacity between the conductive film and the lower layer can be small, whereby radio-frequency signals can be used.

The above-described object is achieved by an electrode structure including a conductive film formed on a base substrate through an insulation film, the insulation film comprising a first film of polyimide having a plurality of openings which reach the base substrate, a second film formed on inside walls of the openings and formed of an insulation material having a higher hardness than polyimide, and a plurality of poles of polyimide buried in

the openings with the second film formed on the inside walls thereof. Because of the second film of an insulation material of a high hardness is formed on the inside walls of the openings formed in the first film of polyimide, even when a strong force is applied upon the bonding, the first film are prevented from being distorted, and the conductive film is protected from peeling off. Because of the thick polyimide layer below the conductive film, a parasitic capacity between the conductive film and the lower layer can be small, whereby radio-frequency signals can be used.

The above-described object is achieved by a semiconductor light-emitting device having an electrode structure including a conductive film formed on a base substrate through an insulation film, the insulation film comprising a plurality of poles of polyimide, a first film formed on side surfaces of the poles and formed of an insulation material having a higher hardness than polyimide, and a second film of polyimide buried among said a plurality of poles with the first film formed on side surfaces thereof. Because of the first film of an insulation material of a high hardness formed on the side surfaces of the poles of polyimide, even when a strong force is applied upon the bonding, the poles are prevented from being distorted, and the conductive film is protected from peeling off. Because of the thick polyimide layer below the conductive film, a parasitic capacity between the

conductive film and the lower layer can be small, whereby radio-frequency signals can be used.

The above-described object is achieved by a semiconductor light-emitting device having an electrode structure including a conductive film formed on a base substrate through an insulation film, the insulation film comprising a first film of polyimide having a plurality of openings which reach the base substrate, a second film formed on inside walls of the openings and formed of an insulation material having a higher hardness than polyimide, and a plurality of poles of polyimide buried in the openings with the second film formed on the inside walls thereof. Because of the second film of an insulation material of a high hardness formed on the inside walls of the openings formed in the first film of polyimide, even when a strong force is applied upon the bonding, the first film is prevented from being distorted, and the conductive film is protected from peeling off. Because of the thick polyimide layer below the conductive film, a parasitic capacity between the conductive film and the lower layer can be small, whereby radio-frequency signals can be used.

The above-described object is achieved by a process for fabricating an electrode structure including a step of forming an insulation film on a base substrate, and a step of forming a conductive film on the insulation film, the step of forming the insulation film comprising a step of

forming a plurality of poles of polyimide on the base substrate, a step of forming on side surface of the poles a first film of an insulation material having a higher hardness than polyimide, and a step of burying a second film of polyimide among the first film. Because of the first film of an insulation material having high hardness formed on the side surfaces of the poles of polyimide, even when a strong force is applied upon the bonding, the poles are prevented from being distorted, and the conductive film is protected from peeling off. Because of the thick polyimide layer below the conductive film, a parasitic capacity between the conductive film and the lower layer can be small, whereby radio-frequency signals can be used.

The above-described object is achieved by a process for fabricating an electrode structure including a step of forming an insulation film on a base substrate and a step of forming a conductive film on the insulation film, the step of forming the insulation film comprising a step of forming on a base substrate a first film of polyimide having a plurality of openings which reach the base substrate, a second step of forming on inside walls of the openings a second film of an insulation material having a higher hardness than polyimide, and a step of forming a plurality of poles of polyimide buried in the openings with the second film formed on the inside walls thereof. Because of the second film of an insulation material of

high hardness is formed on the inside walls of the openings formed in the first film of polyimide, even when a strong force is applied upon the bonding, the poles are prevented from being distorted, and the conductive film is protected from peeling off. Because of the thick polyimide layer below the conductive film, a parasitic capacity between the conductive film and the lower layer can be small, whereby radio-frequency signals can be used.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a perspective view of the semiconductor light-emitting device according to a first embodiment of the present invention.

FIG. 2A is a sectional view of the semiconductor light-emitting device according to the first embodiment of the present invention, which shows a vicinity of the bonding pad.

FIG. 2B is a plan view of the semiconductor light-emitting device according to the first embodiment of the present invention, which shows a vicinity of the bonding pad.

FIG. 3A and 3B are sectional views of the semiconductor light-emitting device according to the first embodiment of the present invention in the steps of the process for fabricating the same, which show the process (Part 1).

FIG. 4A and 4B are sectional views of the semiconductor light-emitting device according to the first embodiment of the present invention in the steps of the process for fabricating the same, which show the process (Part 2).

FIG. 5 is a sectional view of the semiconductor light-emitting device according to the first embodiment of the present invention in the steps of the process for fabricating the same, which shows the process (Part 3).

FIG. 6A is a sectional view of the semiconductor light-emitting device according to a first modification of the first embodiment of the present invention, which shows a vicinity of the bonding pad.

FIG. 6B is a plan view of the semiconductor light-emitting device according to a first modification of the first embodiment of the present invention, which shows a vicinity of the bonding pad.

FIG. 7A is a sectional view of the semiconductor light-emitting device according to a second modification of the first embodiment of the present invention, which shows a vicinity of the bonding pad.

FIG. 7B is a plan view of the semiconductor light-emitting device according to a second modification of the first embodiment of the present invention, which shows a vicinity of the bonding pad.

FIG. 8A is a sectional view of the semiconductor

light-emitting device according to the second embodiment of the present invention, which shows a vicinity of the bonding pad.

FIG. 8B is a plan view of the semiconductor light-emitting device according to the second embodiment of the present invention, which shows a vicinity of the bonding pad.

FIG. 9A and 9B are sectional views of the semiconductor light-emitting device according to the second embodiment of the present invention in the steps of the process for fabricating the same, which show the process (Part 1).

FIG. 10A and 10B are sectional views of the semiconductor light-emitting device according to the second embodiment of the present invention in the steps of the process for fabricating the same, which show the process (Part 2).

FIG. 11 is sectional views of the semiconductor light-emitting device according to the second embodiment of the present invention in the steps of the process for fabricating the same, which shows the process (Part 3).

FIG. 12A is a sectional view of the semiconductor light-emitting device according to a first modification of the second embodiment of the present invention, which shows a vicinity of the bonding pad.

FIG. 12B is a plan view of the semiconductor light-

emitting device according to a first modification of the second embodiment of the present invention, which shows a vicinity of the bonding pad.

FIG. 13 is a plan view of the semiconductor light-emitting device according to a second modification of the second embodiment of the present invention, which shows a vicinity of the bonding pad.

FIG. 14 is a conceptual view showing distortion of the polyimide layer upon the bonding.

DETAILED DESCRIPTION OF THE INVENTION

[A First Embodiment]

The semiconductor light-emitting device according to a first embodiment of the present invention will be explained with reference to FIGS. 1 to 5. FIG. 1 is a perspective view of the semiconductor light-emitting device according to the present embodiment. FIG. 2A is a sectional view of a vicinity of bonding pad, specifically along the line A-A' in FIG. 1. FIG. 2B is a plan view of the vicinity of the bonding pad. In FIG. 2B some constituent members are not shown. FIGS. 3A to 5 show sectional views of the semiconductor light-emitting device according to the present embodiment, which show the process for fabricating the semiconductor light-emitting device.

(Semiconductor Light-emitting Device)

First, the semiconductor light-emitting device

according to the present embodiment will be explained with reference to FIG. 1. In the present embodiment, the present invention is applied to a light-emitting device, but the present invention is applicable not only to semiconductor light-emitting devices, but also widely to all semiconductor devices in which strong forces are applied to the electrodes, such as the bonding pads, etc., when bonded.

As shown in FIG. 1, a guide layer 12 is formed on a substrate 10 of InP. An MQW light absorption layer 14a and a MQW active layer 14b are formed on the guide layer 12. A clad layer 16 is formed on the MQW light absorption layer 14a and the MQW active layer 14b. A clad layer 17 is formed on the clad layer 16. A cap layer 18a, 18b is formed on the clad layer 17. The cap layer 18a, 18b is absent in an isolation region 22 and isolated from each other in the isolation region 22. An electrode 8 of an Au/Ge/Au film is formed on the back side of the substrate 10.

The cap layer 18a, 18b, the clad layers 17, 16, the MQW active layer 14b, the MQW light absorption layer 14a, the guide layer 12 and the substrate 10 are mesa-etched, and a mesa-shaped waveguide is formed. A high-resistance buried layer 30 of InP is formed on both sides of the mesa-shaped waveguide.

A silicon oxide film 32 is formed on the

high-resistance buried layer 30. The silicon oxide film 32 is formed also on the clad layer 17 in the isolation region 22.

Electrodes 24a, 24b of an Au/Pt/Ti film are formed respectively on the cap layer 18a, 18b. The electrodes 24a, 24b are absent in the isolation region 22. Accordingly, a modulator region 26 and a DFB (Distributed FeedBack) laser region 28 are electrically isolated from each other by the isolation region 22.

In the modulator region 26 there are formed polyimide layers 36, 40 and a silicon nitride film 38 which will be described later. A bonding pad 24c is formed on the polyimide layers 36, 40 and the silicon nitride film 38. The bonding pad 24c is connected to the electrode 24a. Because of the polyimide layer 36, etc., which are formed thick, a parasitic capacity between the bonding pad 24c and the lower layer can be small, which allows modulation radio-frequencies to be used.

In the DFB laser region 28, a bonding pad 24d is formed on the silicon oxide film 32. The bonding pad 24d is connected to the electrode 24b. No radio-frequency signal is used in the DFB laser region 28, and it is not necessary to consider a parasitic capacity between the bonding pad 24d and the lower layer.

Then, a structure of the vicinity of the bonding pad 24c of the modulate region 26 will be explained with

reference to FIG. 2. FIG. 2A is a sectional view of the vicinity of the bonding pad 24c and specifically a sectional view of the vicinity along the line A-A' in FIG. 1. FIG. 2B is a plan view of the vicinity of the bonding pad 24c.

As shown in FIG. 2A, the high-resistance buried layer 30 is formed on the substrate 10. A 300 nm-thickness silicon oxide film 32 is formed on the high-resistance buried layer 30. A 200 nm-thickness silicon nitride film 34 is formed on the silicon oxide film 32.

The polyimide layer 36 is formed in a plurality of cylindrical patterns on the silicon nitride film 34. The cylindrical polyimide layer 36 may have, e.g., a 2 μ m-height. In the present embodiment the polyimide layer 36 is used because the polyimide layer 36 is not damaged by impacts of the bonding, etc. because of its high flexibility. In a case that a layer, as of silicon oxide film or others, having low flexibility is formed thick below the bonding pad 24c, the silicon oxide film or others is damaged by impacts of the bonding because of its low flexibility.

The silicon nitride film 34 is formed in a 300 nm-thickness on the entire surface of the silicon nitride film 34 with the polyimide layer 36 formed in a plurality of cylindrical patterns formed on. The silicon nitride film 38 is formed on the sides of the cylindrical patterns

of the polyimide layer 36. The silicon nitride film 38, the hardness of which is higher than that of polyimide, can keep the polyimide layer 36 from being distorted even when a strong force is applied to the bonding pad 24c by the bonding. The silicon nitride film 38, the hardness of which is high, is formed to be as thin as 300 nm and is never damaged by impacts of the bonding.

The polyimide layer 40 is further formed on the silicon nitride film 38. The polyimide layer 40 is as thin as, e.g., about 100 nm above the cylindrical polyimide layer 36. A silicon nitride film 42 is formed on the entire surface of the polyimide layer 40, and the bonding pad 24c is formed on the silicon nitride film 42.

As described above, according to the present embodiment, the silicon nitride film 38, the hardness of which is high, is formed on the sides of the polyimide layer 36 formed in a plurality of cylindrical patterns can prevent the polyimide layer 36 from being distorted even when a strong force is applied to the bonding pad 24c upon the bonding. Because of the polyimide layers 36, 40 formed thick below the bonding pad 24c, a parasitic capacity between the bonding pad 24c and the lower layer can be small, which permits modulation radio-frequencies to be used, whereby according to the present embodiment, a semiconductor light-emitting device using modulation radio-frequencies can be provided.

(Process for Fabricating the Semiconductor Light-emitting Device)

Then, the process for fabricating the semiconductor light-emitting device according to the present embodiment will be explained with reference to FIGs. 3A to 5.

First, the guide layer 12, the MQW light absorption layer 14a, the MQW active layer 14b, the clad layer 16, the clad layer 17 and the cap layer 18a, 18b are sequentially formed on a substrate 10 of InP.

Next, the cap layer 18a, 18b, the clad layers 17, 16, the MQW active layer 14b, the MQW light absorption layer 14a, the guide layer 12 and the substrate 10 are mesa-etched. Then, the high resistance buried layer 30 of InP is formed on both sides of the mesa.

Next, the cap layer 18a, 18b is patterned to be isolated by the isolation region 22.

Then, the silicon oxide film 32 of a 300 nm-thickness is formed on the entire surface by CVD (Chemical Vapor Deposition). Then, the silicon nitride film 34 of a 200 nm-thickness is formed on the silicon oxide film 32 by CVD.

Next, the polyimide layer 36 is formed on the entire surface of the silicon nitride film 34 by spin coating. Next, the polyimide layer 36 is solidified by a heat treatment of about 400 °C. Thus the polyimide layer 36 of an about 2 μ m-thickness is formed (see FIG. 3A).

Then, the polyimide layer 36 is patterned into

cylindrical patterns by photolithography. A diameter of the cylinders may be, e.g., 5 μm , and an interval between each cylinder and its adjacent one may be, e.g., 10 μm . The polyimide layer 36 may be patterned by, dry etching using plasma discharge. An etching gas may be a mixed gas of CF_4 gas and O_2 gas. One hundred, for example, cylinders of the polyimide layer 36 are formed in a 100 μm x 100 μm area near the bonding pad 24c (see FIG. 3B).

Then, the silicon nitride film 38 is formed on the entire surface in a 300 nm-thickness by CVD (see FIG. 4A).

Then, the polyimide layer 40 is formed on the entire surface by spin coating. In the present embodiment the polyimide layer 36 is formed in cylinders, which makes it difficult for the surface of the polyimide layer 40 to be uneven when the polyimide layer 40 is formed. The polyimide layer 40 can have the surface evened. Then, a heat treatment of about 400 $^{\circ}\text{C}$ to solidify the polyimide layer 40. The polyimide layer 40 has an about 100 nm-thickness on the polyimide layer 36 in cylinders (see FIG. 4B).

Then, the silicon nitride film 42 is formed on the entire surface in a 200 nm-thickness by CVD.

Next, an opening which reaches the cap layers 18a, 18b (see FIG. 1) are formed. The opening is for connecting the electrodes 24a, 24c to the cap layer 18a, 18b.

Then, as shown in FIG. 5, a 100 nm-thickness Ti film,

a 70 nm-thickness Pt film and a 500 nm-thickness Au film are sequentially formed on the silicon nitride film 42 by vapor deposition to form the electrodes 24a, 24b and the bonding pads 24c, 24d of the Au/Pt/Ti film. Thus, the semiconductor light-emitting device according to the present embodiment is fabricated (see FIG. 5).

(A First Modification)

Then, a first modification of the semiconductor light-emitting device according to the present embodiment will be explained with reference to FIGs. 6A and 6B. FIG. 6A is a sectional view of the vicinity of the bonding pad. FIG. 6B is a plan view of the vicinity of the bonding pad of the semiconductor light-emitting device according to the present modification. In FIG. 6B some constituent members are omitted.

As shown in FIGs. 6A and 6B, the semiconductor light-emitting device according to the present modification is characterized mainly in that the polyimide layer 36a is formed in quadrangular poles.

In the present modification, when the polyimide layer 36a is patterned, square patterns may be formed. In the semiconductor light-emitting device according to the present embodiment shown in FIG. 2 wherein the polyimide layer 36 is formed in cylinders, it is necessary to form circular patterns and etch the polyimide layer 36, but simply in the present modification quadrangular patterns

may be formed. In consideration of achievement of pattern drawing apparatuses it is difficult to form micronized circular patterns, but it is easy to form micronized quadrangular patterns.

Thus, the semiconductor light-emitting device according to the present modification can be micronized.

(A Second Modification)

Then, a second modification of the semiconductor light-emitting device according to the present embodiment will be explained with reference to FIGs. 7A and 7B. FIG. 7A is a sectional view of the vicinity of the bonding pad of the semiconductor light-emitting device according to the present modification. FIG. 7B is a plan view of the vicinity of the bonding pad of the semiconductor light-emitting device according to the present modification. In FIG. 7B some constituent members are omitted.

As shown in FIG. 7A, the semiconductor light-emitting device according to the present modification is characterized mainly in that the polyimide layer 36 is formed in hexagonal poles.

In the present modification, because the polyimide layer 36b is formed in hexagonal poles, the sections of the silicon nitride film 38 along the substrate 10 are hexagonal. According to the present modification, the silicon nitride film 38 can have higher resistance to a force applied by the bonding.

[A Second Embodiment]

The semiconductor light-emitting device according to a second embodiment of the present invention and the process for fabricating the same will be explained with reference to FIGS. 8A to 11. FIG. 8A is a sectional view of a vicinity of bonding pad of the semiconductor light-emitting device according to the present embodiment. FIG. 8B is a plan view of a vicinity of bonding pad of the semiconductor light-emitting device according to the present embodiment. FIGS. 9A to 11 are sectional views of the semiconductor light-emitting device according to the present embodiment in the steps of the process for fabricating the same, which show the process. The same members of the present embodiment as those of the semiconductor light-emitting device according to the first embodiment and the process for fabricating the same shown in FIGS. 1 to 7B are represented by the same reference numbers not to repeat or to simplify their explanation.

The semiconductor light-emitting device according to the present embodiment is characterized mainly in that silicon nitride film 38 is formed on the inside walls of openings formed in a polyimide layer 36c.

As shown in FIG. 8A, a plurality of the openings 44 which reach the silicon nitride film 34 are formed in the polyimide layer 36c. A sectional shape of the openings 44 along a substrate 10 is circular.

The silicon nitride film 38 is formed on the entire surface of the polyimide layer 36c with the openings 44 thus formed in. The silicon nitride film 38 is formed also on the inside walls of the openings 44. Because the silicon nitride film 38 is formed on the inside walls of the openings 44, even when a strong force is applied to the bonding pad 24c, the polyimide layer 36c is prevented from being distorted.

A polyimide layer 40 is formed on the entire surface of the silicon nitride film 38. The polyimide layer 40 is buried in the openings 44 with the silicon nitride film 38 formed on. On the polyimide layer 40 there are sequentially formed a silicon nitride film 42 and a bonding pad 24c.

As described above, according to the present embodiment, because the silicon nitride film 38, the hardness of which is high, is formed on the inside walls of a plurality of openings 44 formed in the polyimide layer 36c, even when a strong force is applied to the bonding pad 24c by the bonding, the polyimide layer 36c is prevented from being distorted, whereby peeling of the bonding pad 24c can be prevented. Because of the thick polyimide layers 36c, 40 formed below the bonding pad 24c, a parasitic capacity between the bonding pad 24c and the lower layer can be small, whereby radio-frequency signals can be used as the modulation signals. Thus, the

semiconductor light-emitting device according to the present embodiment can have modulation radio-frequencies.

(Process for Fabricating the Semiconductor Light-emitting Device)

Then, the process for fabricating the semiconductor light-emitting device according to the present embodiment will be explained with reference to FIGs. 9A to 11.

The step of forming the silicon nitride film 34 and the steps up to the silicon nitride film forming step are the same as those of the process for fabricating the semiconductor light-emitting device according to the first embodiment shown in FIG. 3A, and are not explained here.

Following step of forming the silicon nitride film 34, the polyimide layer 36c is formed on the entire surface of the silicon nitride film 34 by spin coating. Then an about 400 °C heat treatment is performed to solidify the polyimide layer 36c. Thus the polyimide layer 36c of an about 2 μm thickness is formed (see FIG. 9A).

Then the openings 44 which reach the silicon nitride film 34 are formed in the polyimide layer 36c by photolithography. A diameter of the openings 44 may be, e.g., 5 μm and may be spaced from each other by, e.g., 15 μm . The openings 44 in the polyimide layer 36c may be formed by, e.g., dry etching using plasma discharges. An etching gas may be a mixed gas of CF_4 gas and O_2 gas. Thus, 49 openings, for example, are formed, e.g., a 100 μm x 100

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μm range near the bonding pad 24c (see FIG. 9B). Preferably large openings 44 are formed in consideration of a surface tension of the polyimide so that the polyimide can intrudes without failure into the openings 44 in a later step.

Then, the silicon nitride film 38 is formed in a 300 nm thickness on the entire surface by CVD (see FIG. 10A).

Then, the polyimide layer 40 is formed on the entire surface by spin coating, and the polyimide layer 40 is buried in the openings 44 with the silicon nitride film 38 formed in. The polyimide layer 40 on the polyimide layer 36c is below, e.g., 300 nm. Then, a heat treatment of about 400 °C is performed to solidify the polyimide layer 40 (FIG. 10B).

Then, the silicon nitride film 42 is formed in a 200 nm thickness on the entire surface by CVD.

Next, an opening which reaches the cap layers 18a, 18b (see FIG. 1) is formed. The opening is for connecting electrodes 24a, 24b to the cap layer 18a, 18b.

Then, the electrodes 24a, 24b of an Au/Pt/Ti film and the bonding pads 24c, 24d are formed on the silicon nitride film 42 by vapor deposition in the same way as in the first embodiment. Thus, the semiconductor light-emitting device according to the present embodiment is fabricated.

(A First Modification)

Then, the semiconductor light-emitting device

according to a first modification of the present embodiment will be explained with reference to FIGs. 12A and 12B. FIG. 12A is a sectional view of a vicinity of the bonding pad of the semiconductor light-emitting device according to the present modification. FIG. 12B is a plan view of the vicinity of the bonding pad of the semiconductor light-emitting device according to the present modification.

The semiconductor light-emitting device according to the present modification is characterized in that the openings 44a are quadrangular.

In the present modification, when the polyimide layer 36d is patterned, quadrangular patterns may be formed. In the semiconductor light-emitting device according to the present embodiment shown in FIG. 8 wherein the polyimide layer 36c is formed in cylinders, it is necessary to form circular patterns and etch the polyimide layer 36c, but simply in the present modification quadrangular patterns may be formed. In consideration of achievement of pattern drawing apparatuses it is difficult to form micronized circular patterns, but it is easy to form micronized quadrangular patterns.

Thus, the semiconductor light-emitting device according to the present modification can be micronized.

(A second Modification)

Then, the semiconductor light-emitting device according to a second modification of the present

embodiment will be explained with reference to FIG. 13. FIG. 13 is a plan view of the vicinity of the bonding pad of the semiconductor light-emitting device according to the present modification. In FIG. 13 some members are not shown.

As shown in FIG. 13, the semiconductor light-emitting device according to the present modification is characterized mainly in that the openings 44b are formed in hexagonal poles.

In the present modification the openings 44b are formed in hexagonal poles, and the sections of the silicon nitride film 38 along the substrate 10 are hexagonal. Accordingly the silicon nitride film 38 can have higher resistance to a force applied by the bonding.

[Modifications]

The present intention is not limited to the above-described embodiment and can cover various modifications.

For example, in the first and the second embodiments the silicon nitride film 38 is formed on the entire surface, but the silicon nitride film 38 may be formed at least on the side walls of the polyimide layers 36 to 36e. The silicon nitride film 38 may be formed at least on the side walls of the polyimide layers 36 to 36e, whereby the polyimide layers 36 to 36e are prevented from being distorted upon the bonding.

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A film formed on the side walls of the polyimide layers 36 to 36b is silicon nitride film in the first embodiment but is not essentially silicon nitride film. The film may be any film having high hardness, e.g., a silicon oxide film, an aluminum oxide film, a polysilicon film or others, as long as the film can prevent from the polyimide layers 36 to 36b from being distorted upon the bonding.

In the second embodiment, silicon nitride film is unessentially formed on the inside walls of the openings 44 to 44b, but is not essential. Any film having high hardness, such as silicon oxide film, aluminum oxide film, polysilicon film or others, may be formed as long as the film can prevent the polyimide layers 36c to 36e from being distorted upon the bonding.

The first and the second embodiments have been explained by means of the semiconductor light-emitting device including the modulator region and the DFB laser region isolated from each other. The present invention may be applicable to a semiconductor light-emitting device including the modulator region which is not isolated. In such case the above-described polyimide layers are formed below the bonding pad formed in the DFB laser region.

In the first and the second embodiments polyimide layers are formed below the bonding pad, but the present invention is applicable to a case wherein polyimide layer

is formed below electrodes for flip chip bonding in place of the bonding pad. In this case the electrodes may be formed not only on a part of the substrate but also on the entire surface, and the above-described polyimide layers may be formed below the electrode formed on the entire surface.

WHAT IS CLAIMED IS:

1. An electrode structure including a conductive film formed on a base substrate through an insulation film, the insulation film comprising a plurality of poles of polyimide, a first film formed on side surfaces of the poles and formed of an insulation material having a higher hardness than polyimide, and a second film of polyimide buried among said a plurality of poles with the first film formed on the side surfaces thereof.

2. An electrode structure including a conductive film formed on a base substrate through an insulation film, the insulation film comprising a first film of polyimide having a plurality of openings which reach the base substrate, a second film formed on inside walls of the openings and formed of an insulation material having a higher hardness than polyimide, and a plurality of poles of polyimide buried in the openings with the second film formed on the inside walls thereof.

3. A semiconductor light-emitting device having an electrode structure including a conductive film formed on a base substrate through an insulation film,

the insulation film comprising a plurality of poles of polyimide, a first film formed on side surfaces of the poles and formed of an insulation material having a higher hardness than polyimide, and a second film of polyimide

buried among said a plurality of poles with the first film formed on side surfaces thereof.

4. A semiconductor light-emitting device according to claim 3, wherein

the first film is also formed on upper surfaces of the poles.

5. A semiconductor light-emitting device having an electrode structure including a conductive film formed on a base substrate through an insulation film,

the insulation film comprising a first film of polyimide having a plurality of openings which reach the base substrate, a second film formed on inside walls of the openings and formed of an insulation material having a higher hardness than polyimide, and a plurality of poles of polyimide buried in the openings with the second film formed on the inside walls thereof.

6. A semiconductor light-emitting device according to claim 5, wherein

the second film is also formed on upper surfaces of the first film.

7. A semiconductor light-emitting device according to any one of claim 3, wherein

the conductive film is formed on the insulation film through a third film of an insulation material.

8. A semiconductor light-emitting device according to any one of claim 5, wherein

the conductive film is formed on the insulation film through a third film of an insulation material.

9. A semiconductor light-emitting device according to any one of claim 3, wherein

the conducting film is a bonding pad.

10. A semiconductor light-emitting device according to any one of claim 5, wherein

the conducting film is a bonding pad.

11. A semiconductor light-emitting device according to any one of claim 3, wherein

the insulation film is formed on a layer formed on the base substrate and formed of a material having a higher hardness than the polyimide.

12. A semiconductor light-emitting device according to any one of claim 5, wherein

the insulation film is formed on a layer formed on the base substrate and formed of a material having a higher hardness than the polyimide.

13. A semiconductor light-emitting device including a waveguide, a lower electrode formed below the waveguide, and an upper electrode formed above the waveguide,

the upper electrode having an electrode structure according to claim 1.

14. A semiconductor light-emitting device including a waveguide, a lower electrode formed below the waveguide, and an upper electrode formed above the waveguide,

the upper electrode having an electrode structure according to claim 2.

15. A semiconductor light-emitting device according to claim 13, further comprising

a high resistance layer formed on a side of the waveguide; and

an electrode structure according to claim 1 formed on the high resistance layer.

16. A semiconductor light-emitting device according to claim 14, further comprising

a high resistance layer formed on a side of the waveguide; and

an electrode structure according to claim 2 formed on the high resistance layer.

17. A process for fabricating an electrode structure including a step of forming an insulation film on a base substrate, and a step of forming a conductive film on the insulation film,

the step of forming the insulation film comprising a step of forming a plurality of poles of polyimide on the base substrate, a step of forming on side surface of the poles a first film of an insulation material having a higher hardness than polyimide, and a step of burying a second film of polyimide among the first film.

18. A process for fabricating an electrode structure including a step of forming an insulation film on a base

substrate and a step of forming a conductive film on the insulation film,

the step of forming the insulation film comprising a step of forming on a base substrate a first film of polyimide having a plurality of openings which reach the base substrate, a second step of forming on inside walls of the openings a second film of an insulation material having a higher hardness than polyimide, and a step of forming a plurality of poles of polyimide buried in the openings with the second film formed on the inside walls thereof.

ABSTRACT OF THE DISCLOSURE

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An electrode structure includes a conductive film 24c formed on a base substrate 10 through an insulation film. The insulation film comprises a plurality of poles 36 of polyimide, a first film 38 formed on the side surfaces of the poles and formed of an insulation material of a high hardness than polyimide, and a second film 40 of polyimide buried among the plural poles with the first film formed on the side surfaces thereof. Because of the first film of an insulation material having high hardness formed on the side surfaces of the poles of polyimide, even when a strong force is applied upon the bonding, the poles are prevented from being distorted, and the conductive film is protected from peeling off. Because of the thick polyimide layer below the conductive film, a parasitic capacity between the conductive film and the lower layer can be small, whereby radio-frequency signals can be used.

FIG.2A

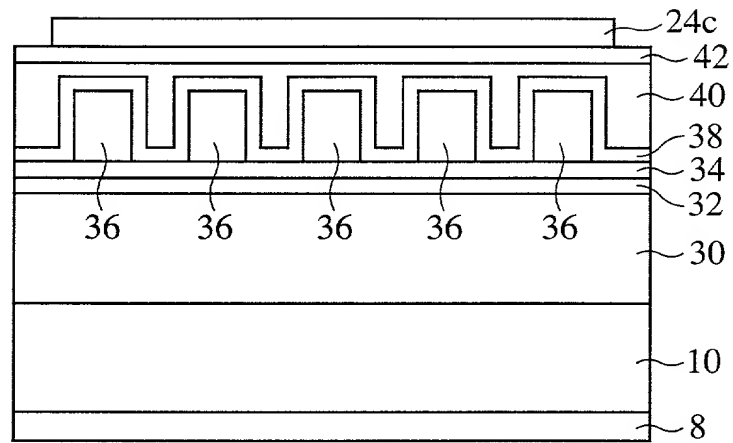


FIG.2B

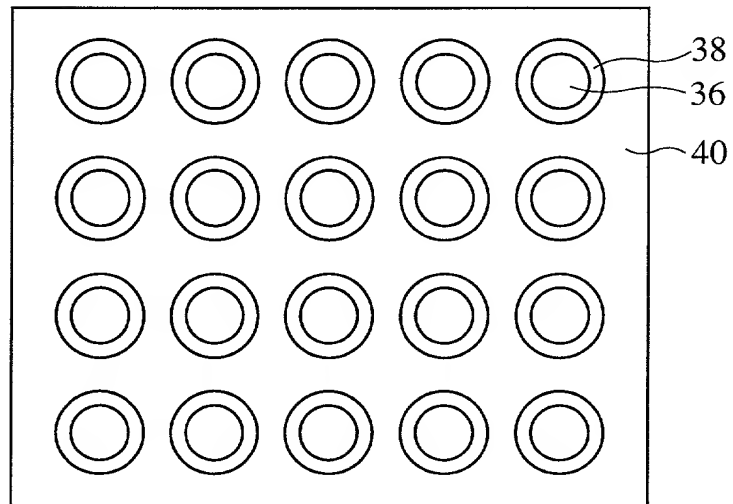


FIG.3A

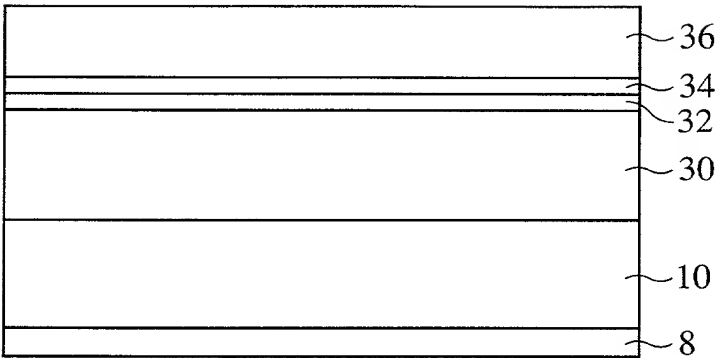


FIG.3B

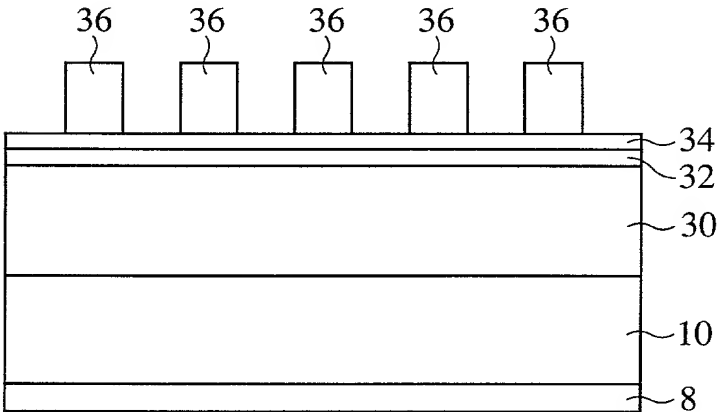


FIG.4A

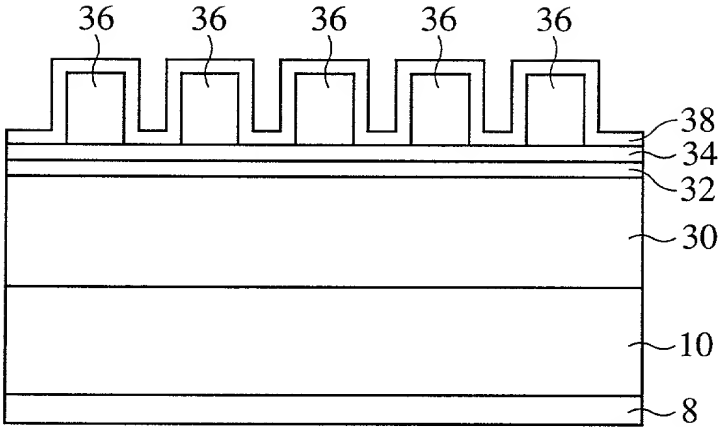


FIG.4B

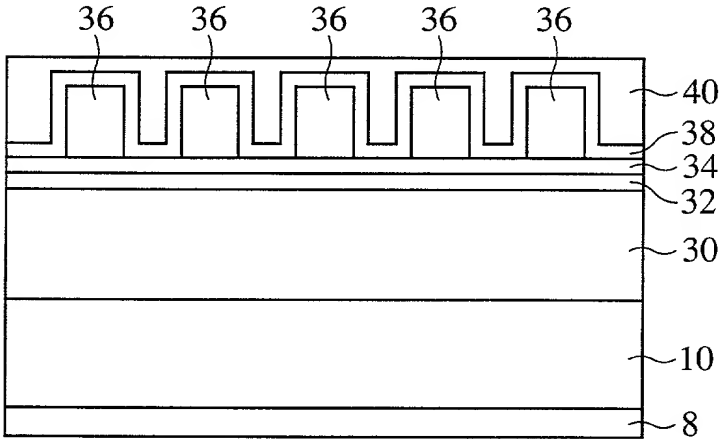


FIG.5

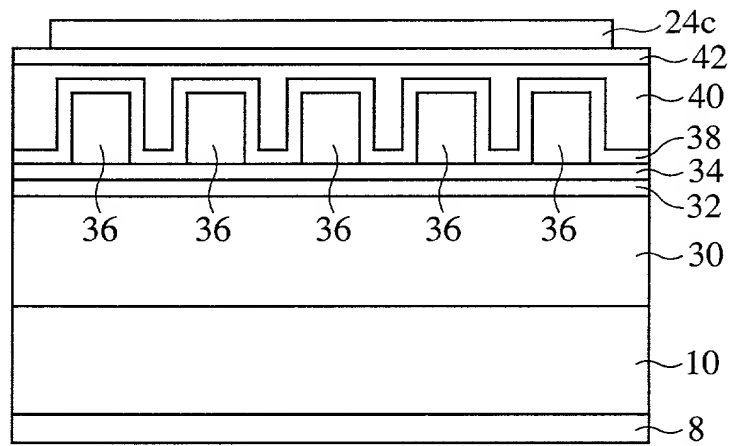


FIG.6A

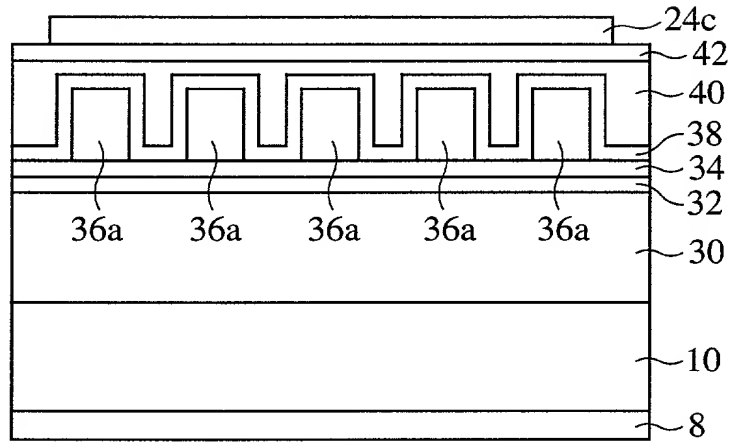


FIG.6B

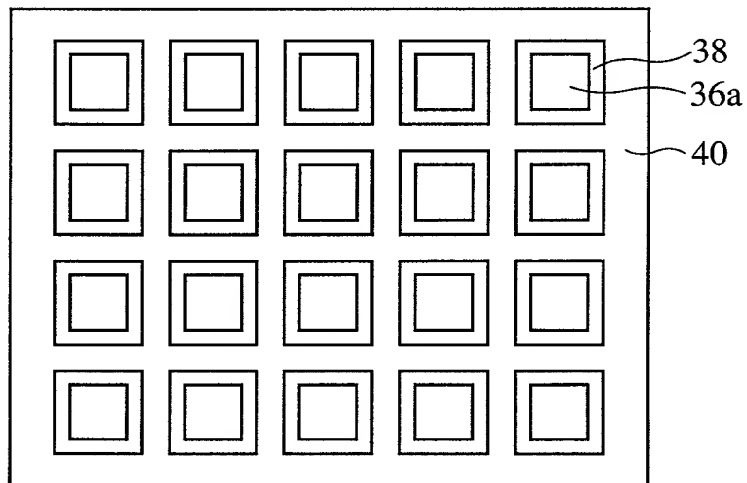


FIG.7A

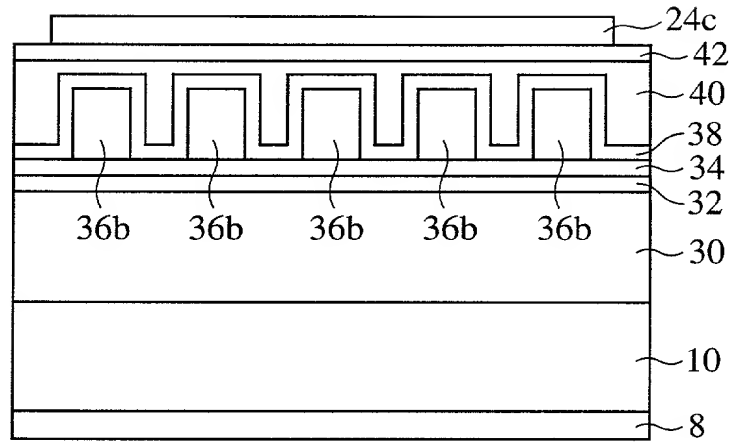


FIG.7B

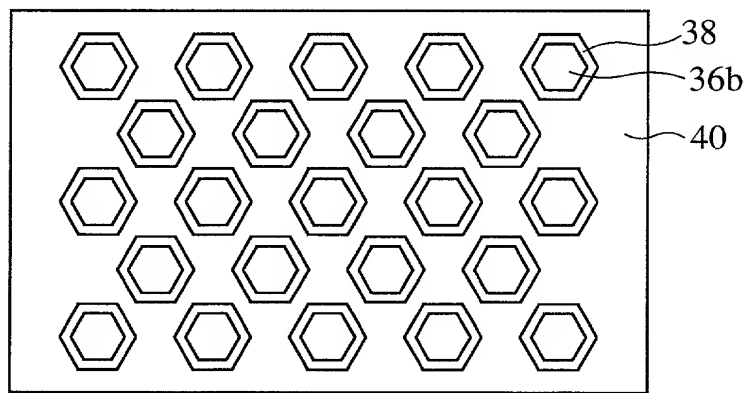


FIG.8A

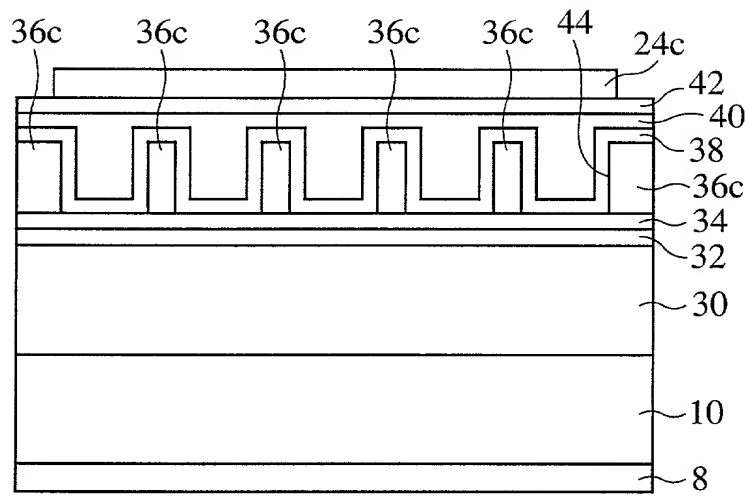


FIG.8B

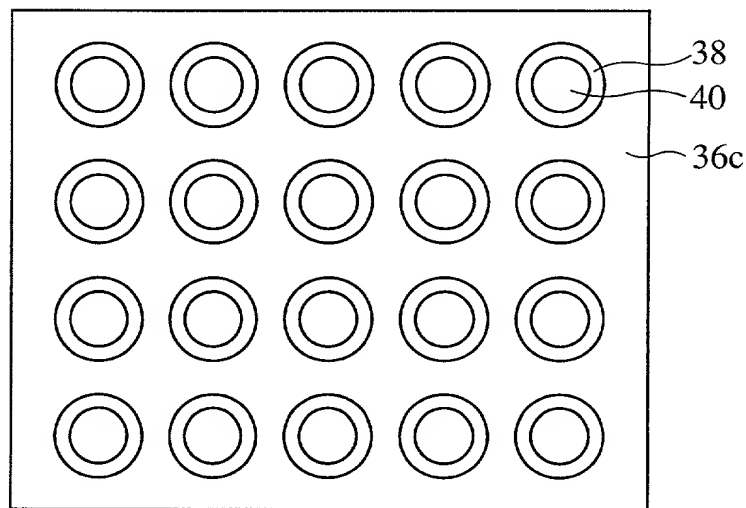


FIG.9A

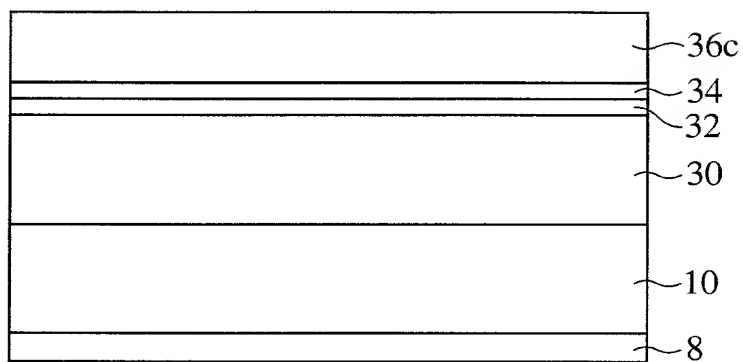


FIG.9B

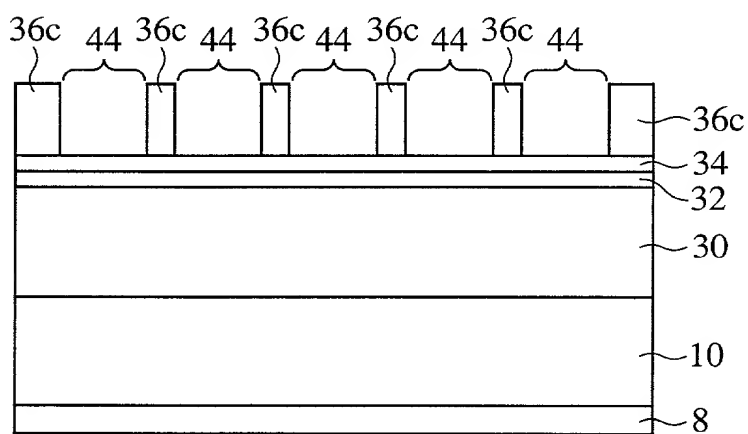


FIG.10A

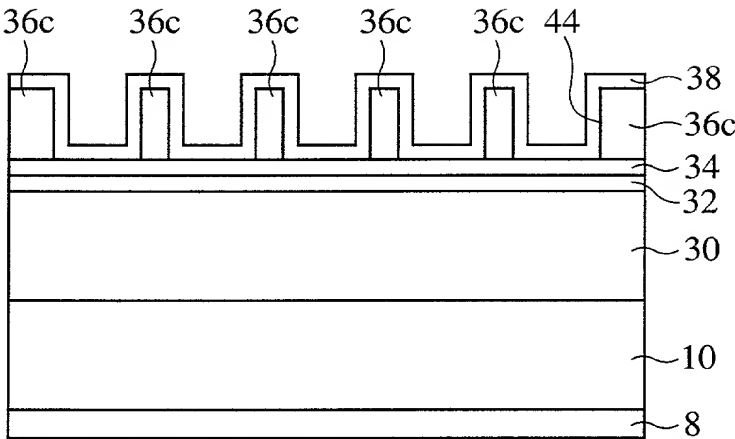


FIG.10B

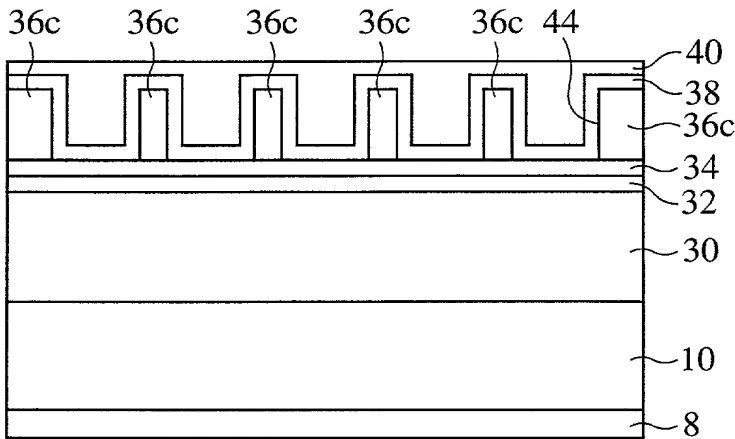


FIG. 11

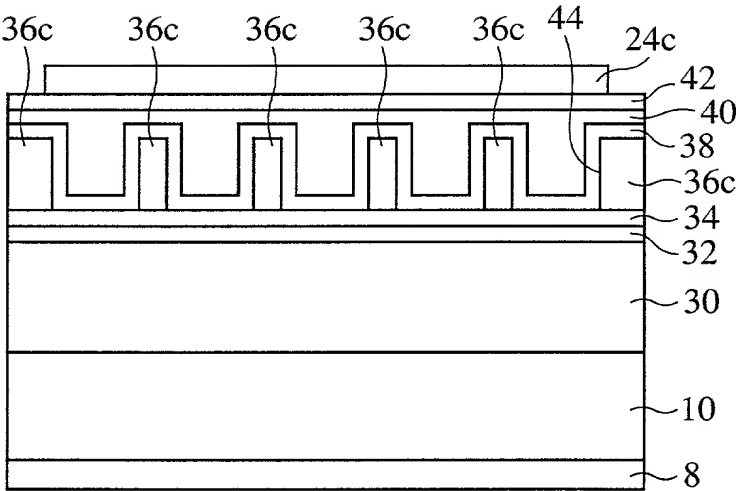


FIG.12A

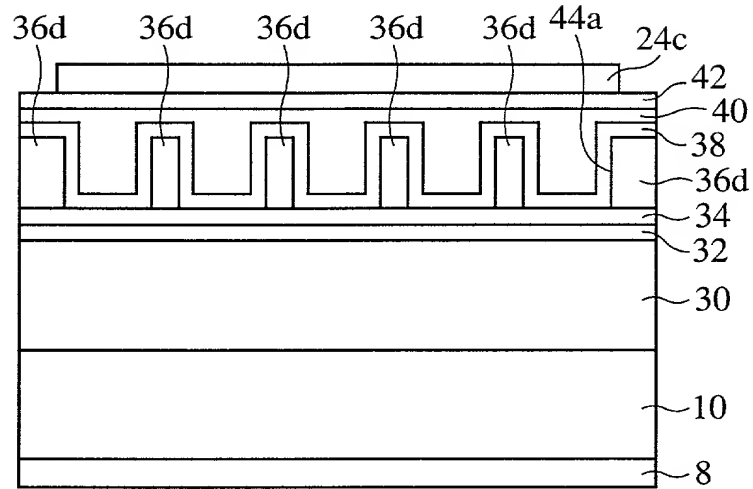


FIG.12B

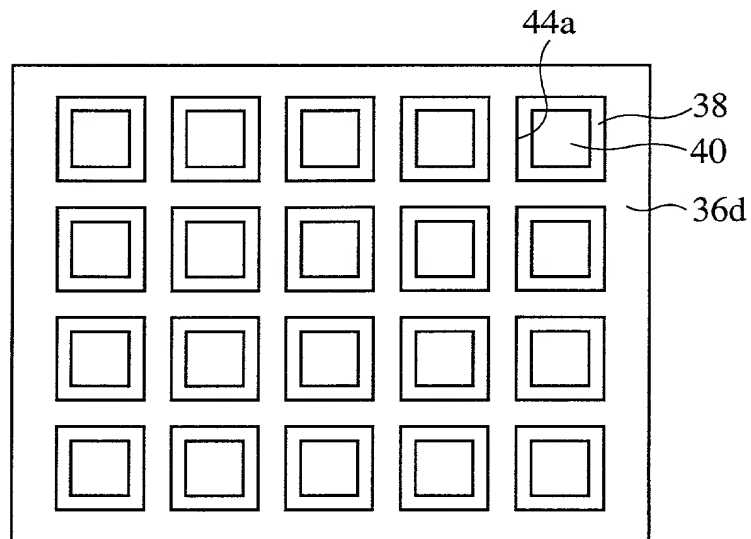


FIG.13

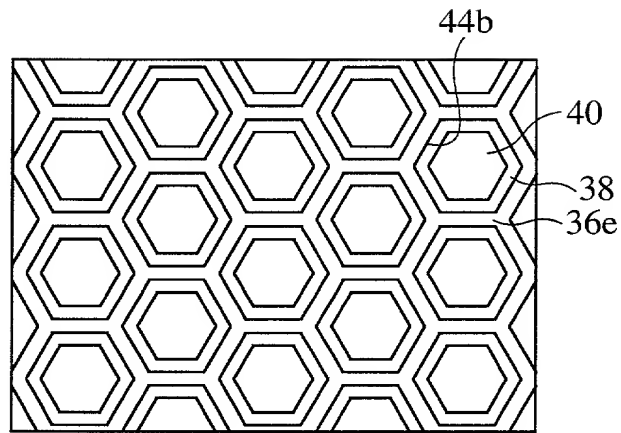
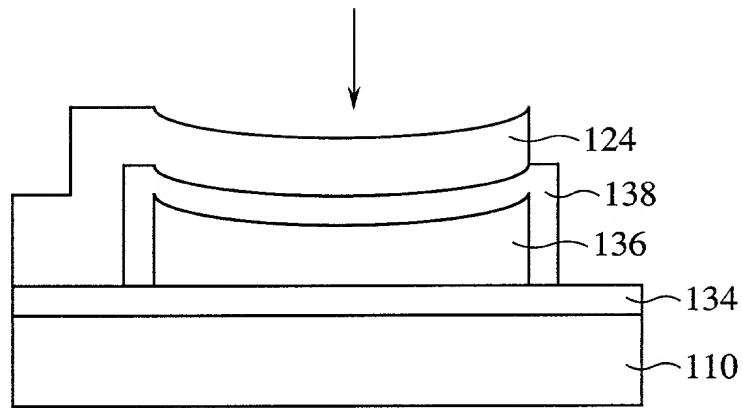


FIG.14



Declaration and Power of Attorney for U.S. Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

ELECTRODE STRUCTURE, PROCESS FOR
FABRICATING ELECTRODE STRUCTURE
AND SEMICONDUCTOR LIGHT-EMITTING
DEVICE

上記発明の明細書（下記の欄でx印がついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

☐ 月 日に提出され、米国出願番号または特許協定条約
国際出願番号を _____ とし、
(該当する場合) _____ に訂正されました。

☐ was filed on _____
as United States Application Number or
PCT International Application Number
_____ and was amended on
_____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37編第1条56項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Japanese Language Declaration (日本語宣言書)

私は、米国法典第35編119条(a)-(d)項又は365条(b)項に基づき下記の、米国外の国の少なくとも一カ国を指定している特許協力条約365(a)項に基づく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

Prior Foreign Application(s)

外国での先行出願

11-73500/1999
(Number)
(番号)

Japan
(Country)
(国名)

(Number)
(番号)

(Country)
(国名)

私と、第35編米国法典119条(e)項に基づいて下記の米国特許出願規定に記載された権利をここに主張いたします。

(Application No.)
(出願番号)

(Filing Date)
(出願日)

私は、下記の米国法典第35編120条に基づいて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約365条(c)に基づき権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第35編112条第1項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第37編1条56項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

(Application No.)
(出願番号)

(Filing Date)
(出願日)

(Application No.)
(出願番号)

(Filing Date)
(出願日)

私は、私自身の知識に基づいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じることに基づく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第18編第1001条に基づき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の表明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Priority Not Claimed

優先権主張なし

March 18, 1999
(Day/Month/Year Filed)
(出願年月日)

☐

(Day/Month/Year Filed)
(出願年月日)

☐

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.)
(出願番号)

(Filing Date)
(出願日)

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

(Status: Patented, Pending, Abandoned)
(現況: 特許許可済、係属中、放棄済)

(Status: Patented, Pending, Abandoned)
(現況: 特許許可済、係属中、放棄済)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration (日本語宣言書)

委任状： 私は下記の発明者として、本出願に関する一切の
手続きを米特許商標局に対して遂行する弁理士または代理人
として、下記の者を指名いたします。(弁理士、または代理
人の氏名及び登録番号を明記のこと)

POWER OF ATTORNEY: As a named inventor, I hereby appoint
the following attorney(s) and/or agent(s) to prosecute this
application and transact all business in the Patent and Trademark
Office connected therewith (list name and registration number)

See list of attorneys and/or agents on page 5.

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Telephone: (202) 659-2930 Fax: (202) 887-0357

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	Japanese		
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	Shinichi Domoto		
第二共同発明者	日付	Second inventor's signature	Date
		Shinichi Domoto	November 24, 1999
住所	Residence		
	Same As Post Office Address		
国籍	Citizenship		
	Japanese		
私書箱	Post Office Address		
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	1000 Kamisukiawara, Oaza, Showa-cho, Nakakoma-gun,		
	Yamanashi-ken 409-3883 Japan		

(第三以降の共同発明者についても同様に記載し、署名をす
ること)

(Supply similar information and signature for third and subsequent
joint inventors.)

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		Nobumasa Okada	
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		Nobumasa Okada	November 24, 1999
住所	Residence		
	Same As Post Office Address		
国籍	Citizenship		
	Japanese		
私書箱	Post Office Address		
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	1000 Kamisukiawara, Oaza, Showa-cho, Nakakoma-gun, Yamanashi-ken 409-3883 Japan		
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国籍	Citizenship		
私書箱	Post Office Address		
第五共同発明者		Full name of fifth joint inventor, if any	
第五発明者の署名	日付	Fifth inventor's signature	Date
住所	Residence		
国籍	Citizenship		
私書箱	Post Office Address		
第六共同発明者		Full name of sixth joint inventor, if any	
第六発明者の署名	日付	Sixth inventor's signature	Date
住所	Residence		
国籍	Citizenship		
私書箱	Post Office Address		

List of attorneys and/or agents

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